

IN THE CLAIMS

What is claimed is:

- 1 1. A data buffering unit, comprising:
2 a memory that stores data from a data transmitting device; and
3 a memory read manager that prepares data stored in the memory for output prior to
4 receiving a request for the data from a data reading device.

- 1 2. The data buffering unit of Claim 1, wherein the memory comprises a plurality of first-
2 in-first-out (FIFO) memories.

- 1 3. The data buffering unit of Claim 2, wherein the memory read manager comprises a
2 memory enable unit that asserts a read enable line to each of the plurality of FIFO memories.

- 1 4. The data buffering unit of Claim 2, wherein the memory read manager comprises a
2 read address manager that determines which of the plurality of FIFO memories to access in
3 response to a read address from the data reading unit.

- 1 5. The data buffering unit of Claim 2, wherein the memory read manager comprises a
2 read selector, coupled to data outputs of each of the FIFO memories, that selects an appropriate
3 data output to receive data from in response to a read address from the data reading device.

- 1 6. The data buffering unit of Claim 2, wherein the memory read manager comprises a
2 plurality of read pointer managers, each corresponding to one of the FIFO memories, the read
3 pointer managers transmit an appropriate read address to each of the FIFO memories to prepare
4 data to be prepared for output on the FIFO memories prior to receiving a request for the data from
5 the data reading device.

1 7. The data buffering unit of Claim 2, further comprising a memory write manager that
2 directs data from the data transmitting device to be written into each of the FIFO memories in a
3 round robin fashion.

1 8. The data buffering unit of Claim 7, wherein the memory write manager comprises a
2 write address manager that determines which of the FIFO memories to access in response to a
3 write address received from the data transmitting device.

1 9. The data buffering unit of Claim 8, wherein the write address manager determines a
2 write address in one of the FIFO memories to write data in response to the write address received
3 from the data transmitting device.

1 10. The data buffering unit of Claim 7, wherein the memory write manager comprises a
2 write selector that transmits a write enable signal and data from the data transmitting device to an
3 appropriate FIFO memory in response to the work address manager.

1 11. A programmable logic device (PLD), comprising,
2 memory blocks that form comprises a plurality of first-in-first-out (FIFO) memories that
3 store data from a data transmitting device; and
4 logic elements that form a memory read manager that prepares data stored in the FIFO
5 memories for output prior to receiving a request for the data from a data reading device.

1 12. The PLD of Claim 11, wherein the memory read manager comprises a memory
2 enable unit that asserts a read enable line to each of the plurality of FIFO memories.

1 13. The PLD of Claim 12, wherein the memory read manager comprises a read address
2 manager that determines which of the plurality of FIFO memories to access in response to a read
3 address from the data reading unit.

1 14. The PLD of Claim 12, wherein the memory read manager comprises a read selector,
2 coupled to data outputs of each of the FIFO memories, that selects an appropriate data output to
3 receive data from in response to a read address from the data reading device.

1 15. The PLD of Claim 12, wherein the memory read manager comprises a plurality of
2 read pointer managers, each corresponding to one of the FIFO memories, the read pointer
3 managers transmit an appropriate read address to each of the FIFO memories to prepare data to be
4 prepared for output on the FIFO memories prior to receiving a request for the data from the data
5 reading device.

1 16. A method for managing data, comprising:
2 selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to
3 output first data stored in a first storage element in the first FIFO memory in response to a first
4 read address from a data reading device; and
5 preparing next data from a next storage element from the first FIFO memory for output.

1 17. The method of Claim 16, wherein the first data was prepared for output by the first
2 FIFO memory prior to a generation of the read address from the data reading device.

1 18. The method of Claim 16, wherein the first data is output within a clock cycle after the
2 first read address from the data reading device is generated.

1 19. The method of Claim 16, wherein preparing the next data from the next storage
2 element from the first FIFO memory to output comprises transmitting a read address of the next
3 storage element to the first FIFO memory prior to a request for the next data from the data
4 reading device.

1 20. The method of Claim 16, further comprising:
2 selecting a second FIFO memory from the plurality of FIFO memories to output second
3 data stored in a first storage element in the second FIFO memory in response to a second read
4 address from the data reading device; and
5 preparing next data from a next storage element from the second FIFO memory for
6 output.

1 21. The method of Claim 20, wherein the selecting the second FIFO memory is
2 performed during the preparing of the next data from the next storage element from the first FIFO
3 memory for output.

1 22. The method of Claim 16, further comprising writing data into the plurality of FIFO
2 memories in a round robin fashion.